TOPIC: SYNTHESIS DESIGN FLOW

Module 4.3 Verilog Synthesis
Verilog design and synthesis flow

In this ppt we will explain:

- Design flow with Verilog
- Verilog Synthesis flow
VLSI Design flow using Verilog

A top-down design starts with a behavioral description and is finally sent to the fab after complete placement, layout and final verification as shown in this diagram on right.
VLSI Design flow

- **Step 1**: Write a high-level behavioral description of the planned design. This step starts with concepts and ends up with a high level description in the Verilog language. This description can have various levels of detail and essentially has architectural elements and algorithmic elements.

- **Step 2**: Next we perform stepwise refinement to the RTL level. This is again simulated and verified for functional correctness.

- **Step 3**: Synthesize the HDL description with the synthesizer. Detail synthesis flow is explained in later part of this ppt.
VLSI Design flow

- **Step 4**: The output of a synthesizer is a gate-level Verilog description. Compare the output of the gate-level simulation (step 3) against the output of the original Verilog description.

- **Step 5**: After this the layout of the design is prepared followed by post-layout verification.
To fully utilize the benefits of logic synthesis, the designer must first understand the flow from the high-level RTL description to a gate-level netlist.
Stage in Synthesis flow

- **RTL description**: The designer describes the design at a high level by using RTL constructs.

- **Translation**: The RTL description is converted by the logic synthesis tool to an unoptimized, intermediate, internal representation.

- **Logic optimization**: The logic is now optimized to remove redundant logic. Various technology independent boolean logic optimization techniques are used.

- **Technology mapping and optimization**: In this step, the synthesis tool takes the internal representation and implements the representation in gates, using the cells provided in the technology library.
Stages in Synthesis flow

- **Technology library**: The technology library contains library cells provided by ABC Inc. The term standard cell library and the term technology library are identical and are used interchangeably.

- **Design constraints**: Design constraints typically include the following:
  - **Timing**: The circuit must meet certain timing requirements. An internal static timing analyzer checks timing.
  - **Area**: The area of the final layout must not exceed a limit.
  - **Power**: The power dissipation in the circuit must not exceed a threshold.
Stages in Synthesis flow

- **Optimized gate-level description:**
  - After the technology mapping is complete, an optimized gate-level netlist described in terms of target technology components is produced.
  - The designer modifies the RTL or reconstrains the design to achieve the desired results. This process is iterated until the netlist meets the required constraints.