Design and FPGA Implementation of High Speed Vedic Multiplier

Sudeep.M.C  
UG Scholar, Dept. of ECE  
Christ University, Bangalore

Sharath Bimba.M  
Asst. Professor, Dept. of ECE  
Christ University, Bangalore

Mahendra Vucha  
Asst. Professor, Dept. of ECE  
Christ University, Bangalore

ABSTRACT
Multiplication is an operation much needed in Digital Signal Processing for various applications. This paper puts forward a high speed Vedic multiplier which is efficient in terms of speed, making use of Urdhva Tiryagbhyam, a sutra from Vedic Math for multiplication and Kogge Stone algorithm for performing addition of partial products and also compares it with the characteristics of existing algorithms. The below two algorithms aids to parallel generation of partial products and faster carry generation respectively, leading to better performance. The code is written in Verilog HDL and implemented on Xilinx Spartan 3 and Spartan 6 FPGA kit using Xilinx ISE 9.1i. The propagation delay of the implemented architecture is obtained to be 28.699ns and 15.752ns respectively.

General Terms
Urdhva Tiryagbhyam Algorithm, Kogge Stone Algorithm, Vedic Multiplier.

Keywords

1. INTRODUCTION
Vedic Mathematics is an ancient system of math practiced during Vedic age which was reconstructed by Jagadguru Swami Sri Bharati Krishna Tirthaji Maharaja[1] between 1911 and 1918 from certain Sanskrit manuscripts. It is perhaps the most refined and efficient mathematical system possible. One of such efficient technique has been employed to enhance the design of a multiplier. Multipliers are the key blocks of a Digital Signal processor. Multiplication is the key aspect, whereby improvement in computational speed of multiplication decreases the processing time of Digital Signal Processors. Convolution, Fast Fourier transforms and various other transforms make use of multiplier blocks.

A faster method for multiplication based on ancient Indian Vedic mathematics is studied in this paper. Among various methods of multiplications in Vedic mathematics, Urdhva Tiryagbhyam is efficient [2]. Urdhva Tiryagbhyam is a general multiplication formula applicable to all cases of multiplication. For addition of partial products in the multiplier Kogge Stone algorithm is used and realized. The code is written in Verilog HDL[3] and synthesized using Xilinx ISE 9.1i and implemented on Spartan 3 and 6 FPGA devices.

2. LITERATURE REVIEW
The algorithms and multiplier architecture was studied from [4, 5, 6, 7, 8, 9, 10, 11] and are represented below.

2.1 Urdhva Tiryagbhyam
Consider ABC as multiplicand and DEF as the multiplier. The steps of multiplication are descriptive in the figure above and the examples are solved below for better understanding.

2.1.1 Illustration:

Figure 1: Illustration of decimal multiplication using Vedic technique

Figure 2: Illustration of binary multiplication using Vedic technique

2.1.2 How is it better than the conventional method?
Figure 3: Difference between Conventional Multiplication and Vedic technique

In conventional method, partial products are summated only after every partial product is obtained. Whereas, in Vedic technique, partial products are obtained vertically as shown in the figure above and simultaneously once all the elements of a column are obtained, respective partial products are added. Hence, leads to advancement in speed over the conventional method.

2.2 Kogge Stone Algorithm

Kogge Stone algorithm was developed by Peter M. Kogge and Harold S. Stone and published in an IEEE seminar in 1973[6]. It generates carry in $O(\log n)$ time and is used in the industry for high performance arithmetic circuits considering it to be the fastest adder. Carries are computed faster using KSA [9, 10, 11] at the cost of increased area.

Figure 4: 16-bit Kogge stone adder network [8]

This is an attempt to apprehend the functioning of KSA in three distinct steps:

1. Pre processing
   This step involves computation of generate and propagate signals corresponding to each pair of bits in A and B. These signals are given by the logic equations below:
   
   $P(i) = A(i) \oplus B(i)$
   
   $G(i) = A(i) \cdot B(i)$

2. Carry look ahead network
   This is the block responsible for advancement in speed. This step involves computation of carries corresponding to each bit. It uses group propagate and generate as intermediate signals which are given by the logic equations below:
   
   $P_i:j = P(i: k + 1) \cdot P(k:j)$
   
   $G_i:j = G(i: k + 1) + (P(i: k + 1) \cdot G(k:j))$

In the Figure 4, Black box represents the computation of both $P_i:j$ and $G_i:j$ whereas grey box represents the computation of $G_i:j$ alone and White triangular objects are buffers.

3. Post processing
   It involves computation of sum bits. Sum bits are computed by the logic given below:

   $S(i) = P(i) \oplus G(i - 1)$

3. PROPOSED MULTIPLIER

Proposed multiplier architecture of 2x2, 4x4, and 8x8 bit VM module are displayed below. The basic architecture was comprehended from the base paper [4] and modified to obtain the right output as well as gain speed. The major change adopted here in the architecture is that we have used Kogge stone algorithm to add partial products rather than RCA, CLA and CSA.

Figure 5: 2x2 Vedic Multiplier

Figure 6: 4x4 Vedic Multiplier using KSA
4. RESULTS AND SIMULATIONS

The Verilog code of 8x8 Vedic multiplier was synthesized using Xilinx ISE 9.1i and was implemented on FPGA device xc3s400-5tq144 of SPARTAN 3 Family. The results are shown below. DIP switches are used as input devices and LEDs are used as output devices. Comparison of delays between 8x8 modified Vedic multipliers using RCA and KSA executed on xc3s700-afg484 and VM using RCA represented in the paper \[4\] are shown in Table 1.

<table>
<thead>
<tr>
<th>Device Utilization Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic Utilization</td>
</tr>
<tr>
<td>Logic Distribution</td>
</tr>
<tr>
<td>Total Number of 4 input LUTs</td>
</tr>
<tr>
<td>Number of logic blocks:</td>
</tr>
<tr>
<td>Number of 8 bit logic blocks</td>
</tr>
<tr>
<td>Number of 8 bit logic blocks containing only related logic</td>
</tr>
<tr>
<td>Number of 8 bit logic blocks containing unrelated logic</td>
</tr>
</tbody>
</table>

4.1 Outputs of Simulation:

4.2 Outputs of Implementation:

1. \(\frac{(11111111)_2-(11111111)_2}{(11111111000000000000)_2}\)

Inputs:

Output:

2. \(\frac{(00111001)_2-(00011001)_2}{(0000010111001000001)_2}\)

Inputs:

Output:
4.3 Comparison

Table 1. Comparison of delay produced by 8x8 VM using RCA and KSA adders.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PROGRAM</th>
<th>DELAY (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VM8x8RCA[4]</td>
<td>[a].</td>
<td>28.27</td>
</tr>
<tr>
<td>VM8x8RCA</td>
<td>[b].</td>
<td>27.586</td>
</tr>
<tr>
<td>VM8x8KSA</td>
<td>[c].</td>
<td>26.178</td>
</tr>
<tr>
<td>[a]-[b]</td>
<td></td>
<td>0.684</td>
</tr>
<tr>
<td>[a]-[c]</td>
<td></td>
<td>2.092</td>
</tr>
<tr>
<td>[b]-[c]</td>
<td></td>
<td>1.408</td>
</tr>
</tbody>
</table>

Table 2. Comparison of delay produced by 8x8 VM on SPARTAN 3 and SPARTAN 6 device.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PROGRAM</th>
<th>DELAY (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>xc3s400-5q144</td>
<td>8x8 Vedic Multiplier</td>
<td>28.699</td>
</tr>
<tr>
<td>xc6slx75t-3fgg676</td>
<td>8x8 Vedic Multiplier</td>
<td>15.752</td>
</tr>
</tbody>
</table>

Table 3. Comparison of delay produced by various 8x8 multipliers.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PROGRAM</th>
<th>DELAY (ns)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Array Multiplier[5]</td>
<td></td>
<td>32.01</td>
</tr>
<tr>
<td>VM8x8KSA</td>
<td></td>
<td>23.644</td>
</tr>
</tbody>
</table>

5. CONCLUSION

By comparing tables 1, 2 and 3 we conclude that the proposed technique of multiplication using UrdhvaTiragbyam algorithm and Kogge Stone algorithm causes less latency when compared to available techniques in literature. The proposed technique when implemented for 8x8 bit multiplication, the delay is found to be 28.699ns on SPARTAN 3 and 15.752 ns on SPARTAN 6. The adoption of KSA algorithm for higher bit size multipliers will further show improvement in speed[9]. Further, higher speeds can be achieved by making use of pipelining and parallel processing techniques. This work will increase awareness of Vedic mathematics techniques in the field of engineering and delivers high performance in DSP Processors.

6. AUTHORS

Sudeep M.C pursuing his B.Tech degree at Christ Faculty of Engineering, Christ University, Bangalore, Karnataka, India. His areas of interest are VLSI Technologies and Embedded systems.

Sharath Bimba M received her B.Tech degree in Electrical and Electronics Engineering from Sri Venkateshwara University, Tirupati, Andhra pradesh, India in 2008 and M.Tech degree in VLSI Systems in 2010 from National Institute of Technology, Trichy, Tamilnadu, India. She is currently working as Asst. Professor in the dept. of ECE, Christ University, Bangalore, India. Her areas of interest are Microelectronics, VLSI systems and Nanotechnology.

Mahendra Vucha received his B.Tech degree in Electronics and Communication engineering from JNTU, Hyderabad in 2007 and M.Tech degree in VLSI and Embedded System Design from MANIT, Bhopal in 2009. He is currently working for his PhD degree at MANIT and also working as Asst.Professor in the Dept. of ECE, Christ University, Bangalore, India. His areas of interest are Hardware Software Co-Design, Analog Circuit design, Digital System Design and Embedded System Design.

7. REFERENCES


